IN THE ABSTRACT

Please replace the present Abstract with the new Abstract as shown on page 3 of this Amendment.

ABSTRACT

The invention relates to fast analogue-to-digital converters having differential inputs and a parallel structure, comprising at least one network of N series resistors with value r and one network of N comparators. The series resistor network receives a reference voltage and is traversed by a fixed current I_0 and the row i (i varying from 1 to N) comparator essentially comprises a dual differential amplifier with four inputs; two inputs receive a differential voltage VS-VN to be converted, a third being connected to a row i resistor of the network, and a fourth input being connected to an N-i row resistor of the network. The resistor network is supplied by a variable reference voltage originating from a servoloop circuit which locks the voltage level of the middle of the resistor network at a voltage equal to the common mode voltage (VS-VSN)/2 present at the output of the sample-and-hold module.